

UNITED STATES PATENT APPLICATION FOR:

# ATOMIC LAYER DEPOSITION APPARATUS

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## CERTIFICATION OF MAILING UNDER 37 C.F.R. 1.10

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## ATOMIC LAYER DEPOSITION APPARATUS

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

**[0001]** The present invention relates to integrated circuit processing equipment and, more particularly to atomic layer deposition (ALD) equipment.

#### Description of the Background Art

**[0002]** Semiconductor wafer processing systems that perform atomic layer deposition (ALD) are used to form material layers on high aspect ratio structures. Referring to FIG. 1, ALD systems typically comprise a deposition chamber 10, a gas supply system 12, and a gas exhaust system 14. The deposition chamber includes a pedestal 11 that is used to support a substrate 13 such as a semiconductor wafer. The gas supply system 12 is used to provide reaction gases to the deposition chamber 10, and the gas exhaust system 14 is used to remove reaction gases from the deposition chamber 10.

**[0003]** In ALD processes, a material layer is formed on a substrate by sequentially chemisorbing alternating monolayers of two or more compounds thereon. Each of the alternating monolayers is chemisorbed onto the substrate by providing a different deposition gas to the chamber that comprises one of the two or more compounds used to form the material layer. After each monolayer is chemisorbed on the substrate, a purge gas is introduced into the deposition chamber to flush the deposition gas therefrom.

**[0004]** Since each of the alternating monolayers of the two or more compounds used to form the material layer is chemisorbed onto the substrate by providing a different deposition gas to the chamber followed by a purge gas, atomic layer deposition (ALD) processes are time consuming. As such, integrated circuit fabrication using ALD processes are costly due to decreased wafer throughput.

**[0005]** Therefore, a need exists in the art for atomic layer deposition (ALD) systems for integrated circuit fabrication.

#### SUMMARY OF THE INVENTION

**[0006]** A method and apparatus for atomic layer deposition (ALD) is described. The apparatus comprises a deposition chamber and a wafer support. The deposition chamber is divided into two or more deposition regions that are integrally connected one to another. The wafer support is movable between the two or more interconnected deposition regions within the deposition chamber.

**[0007]** The atomic layer deposition (ALD) apparatus is compatible with integrated circuit fabrication processes. In one integrated circuit fabrication process, a substrate is positioned on a wafer support in an ALD apparatus comprising two or more integrally connected deposition regions. The wafer support with the substrate thereon is then moved into a first one of the integrally connected deposition regions wherein a first monolayer of a first compound is formed on the surface thereof. After the first monolayer of the first compound is formed on the surface of the substrate the wafer support is moved to a second one of the integrally connected deposition regions wherein a second monolayer of a second compound is formed on the first monolayer of the first compound. Thereafter, alternate monolayers of the first and second compounds are deposited one over the other by moving the wafer support with the substrate thereon between the two or more integrally connected deposition regions until a material layer having a desired thickness is formed on the substrate.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0008]** The teachings of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

**[0009]** FIG. 1 is a schematic diagram of a prior art atomic layer deposition (ALD) apparatus;

**[0010]** FIG. 2 is a schematic diagram of an atomic layer deposition (ALD) apparatus that can be used for the practice of embodiments described herein; and

**[0011]** FIG. 3 is a flow diagram of a process sequence for the atomic layer deposition (ALD) apparatus of FIG. 2.

#### DETAILED DESCRIPTION

**[0012]** FIG. 2 is perspective view of an atomic layer deposition (ALD) apparatus 100 that can be used to form a material layer on a semiconductor substrate in accordance with embodiments described herein. The ALD apparatus 100 comprises a deposition chamber 105, a gas panel 130, a control unit 110, along with other hardware components such as power supplies 106 and vacuum pumps 102.

**[0013]** The deposition chamber 105 comprises two or more deposition regions 200, 300 that are integrally connected to each other. In FIG. 2 the two or more deposition regions 200, 300 are configured as one above the other in a vertical arrangement, however it is contemplated that the two or more deposition regions may also be configured in a side by side horizontal arrangement (not shown).

**[0014]** The two or more deposition regions 200, 300 are integrally connected one to another with an aperture 250. The aperture 250 is of a sufficient size to permit the passage therethrough of a wafer support 150 having a substrate thereon.

**[0015]** The aperture 250 is optionally sealed. The aperture is sealed to minimize the intermixing of deposition gases within the two or more deposition regions 200, 300. Physical and/or pressure differences may be used.

**[0016]** Alternatively, an inert gas flow may be used to minimize the intermixing of deposition gases at the aperture 250 between the two or more deposition regions 200, 300. The inert gas flow provides a laminar flow

around the area of the aperture 250. The inert gas flow is provided around the area of the aperture 250 through orifices (not shown).

**[0017]** The process chamber 105 houses a wafer support 150, which is used to support a substrate such as a semiconductor wafer 190. The wafer support 150 is moveable inside the chamber 105 between the integrally connected deposition regions 200, 300 using a displacement mechanism (not shown).

**[0018]** Depending on the specific process, the semiconductor wafer 190 can be heated to some desired temperature prior to material layer deposition. For example, wafer support 150 may be heated by an embedded heater element 170. The wafer support 150 may be resistively heated by applying an electric current from an AC power supply 106 to the heater element 170. The wafer 190 is, in turn, heated by the wafer support 190.

**[0019]** A temperature sensor 172, such as a thermocouple, may also be embedded in the wafer support 150 to monitor the temperature of the support in a conventional manner. The measured temperature can be used in a feedback loop to control the power supplied to the heater element 170, such that the wafer temperature can be maintained or controlled at a desired temperature which is suitable for the particular process application. The pedestal may optionally be heated using radiant heat (not shown).

**[0020]** A vacuum pump 102 is used to evacuate each of the deposition regions 200, 300 of the process chamber 105 and to maintain the proper gas flows and pressure inside the chamber 105. Orifices 120 provide process gases to each of the one or more deposition regions 200, 300. Each orifice 120 is connected to a gas panel 130 via a gas line 125, which controls and supplies various gases used in different steps of the deposition sequence.

**[0021]** Proper control and regulation of the gas flows through the gas panel 130 is performed by mass flow controllers (not shown) and the control unit 110. Illustratively, the control unit 110 comprises a central processing unit (CPU) 113, as well as support circuitry 114, and memories containing associated control software 116. The control unit 110 is responsible for automated control of the numerous steps required for wafer processing - such as movement of the wafer support, gas flow control, temperature control,

chamber evacuation, and other steps. Bi-directional communications between the control unit 110 and the various components of the ALD 100 are handled through numerous signal cables collectively referred to as signal buses 118, some of which are illustrated in FIG. 2.

**[0022]** The central processing unit (CPU) 113 may be one of any form of general purpose computer processor that can be used in an industrial setting for controlling process chambers as well as sub-processors. The computer may use any suitable memory, such as random access memory, read only memory, floppy disk drive, hard drive, or any other form of digital storage, local or remote. Various support circuits may be coupled to the CPU for supporting the processor in a conventional manner. Process sequence routines as required may be stored in the memory or executed by a second CPU that is remotely located.

**[0023]** The process sequence routines are executed after the substrate 190 is positioned on the wafer support 150. The process sequence routines, when executed, transform the general purpose computer into a specific process computer that controls the chamber operation so that the deposition process is performed. Alternatively, the chamber operation may be controlled using remotely located hardware, as an application specific integrated circuit or other type of hardware implementation, or a combination of software and hardware.

**[0024]** Referring to FIG. 3, the ALD process sequence begins when a semiconductor wafer is positioned on the wafer support in one of the two or more deposition regions 200, 300 of the deposition chamber 105, as indicated in step 350.

**[0025]** After the semiconductor wafer is positioned on the wafer support, a deposition gas is provided to each of the two or more deposition regions 200, 300, as indicated in step 360 of FIG. 3. A different deposition gas is provided to each of the two or more deposition regions 200, 300. The deposition gases may each be provided using a continuous flow, or optionally using a pulsed flow.

**[0026]** Thereafter as indicated in step 370 of FIG. 3, alternating monolayers of each deposition gas are chemisorbed onto the surface of the

semiconductor wafer to form a material layer having a desired thickness thereon. Each monolayer is chemisorbed onto the surface of the semiconductor wafer as the wafer support is alternately moved between the two or more deposition regions through aperture 250.